element formation region, said partial isolation region including a partial insulating film provided in an upper layer portion of said SOI layer and a partial insulating film lower semiconductor region to be a part of said SOI layer present in a lower layer portion of said SOI layer,

said MOS transistor including:

source and drain regions of a first conductivity type selectively formed in said SOI layer, respectively;

a gate electrode having a gate electrode main part formed through a gate oxide film on a region of said SOI layer between said source and drain regions; and

a body region having a body region main part to be a region of a second conductivity type of said SOI layer between said source and drain regions and a body region potential setting portion electrically connected from said body region main part in said element formation region and capable of externally fixing an electric potential,

wherein said body region potential setting section includes a body region source/drain adjacent portion in a gate width direction adjacently to said source and drain regions and extended in a gate length direction from said body region main part,

said gate electrode further includes a gate extension region extended in said gate length direction from an end of said gate electrode main part and formed on a part of said body region source/drain adjacent portion, and serving to electrically block said body region source/drain adjacent portion and said source and drain regions through said gate extension region, and

a thickness of said partial insulating film lower semiconductor region is thinner than a thickness of said source and drain regions.

3. (Amended) The semiconductor device according to claim 1, wherein

said body region source/drain adjacent portion includes a first body region source/drain adjacent portion extended in a first direction from said body region main part and a second body region source/drain adjacent portion extended in a second direction opposite to said first direction from said body region main part, and

said gate extension region includes a first gate extension region formed on a vicinity of said first body region source/drain adjacent portion and a second gate extension region extended on a vicinity of said second body region source/drain adjacent portion.

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4. (Amended) The semiconductor device according to claim 1, wherein

said body region source/drain adjacent portion includes one body region source/drain adjacent portion, and

said gate extension region includes one gate extension region formed on a vicinity of said body region source/drain adjacent portion.

5. (Amended) The semiconductor device according to claim 1, wherein

said body region source/drain adjacent portion has a high concentration region having a higher impurity concentration of a second conductivity type than that in other regions over a region provided apart from said gate extension region by a predetermined distance.

6. (Amended) The semiconductor device according to claim 1, wherein

said gate extension region includes a gate extension region having an impurity concentration of the second conductivity type of 5×10^{18} cm $^{-3}$ or less.

REMARKS

Favorable reconsideration of this application, in light of the present amendments and following discussion, is respectfully requested. Claims 1, 3, and 8-12 are presently active; Claim 2 has been cancelled; Claims 4-7 and 13-20 have been withdrawn from consideration;